

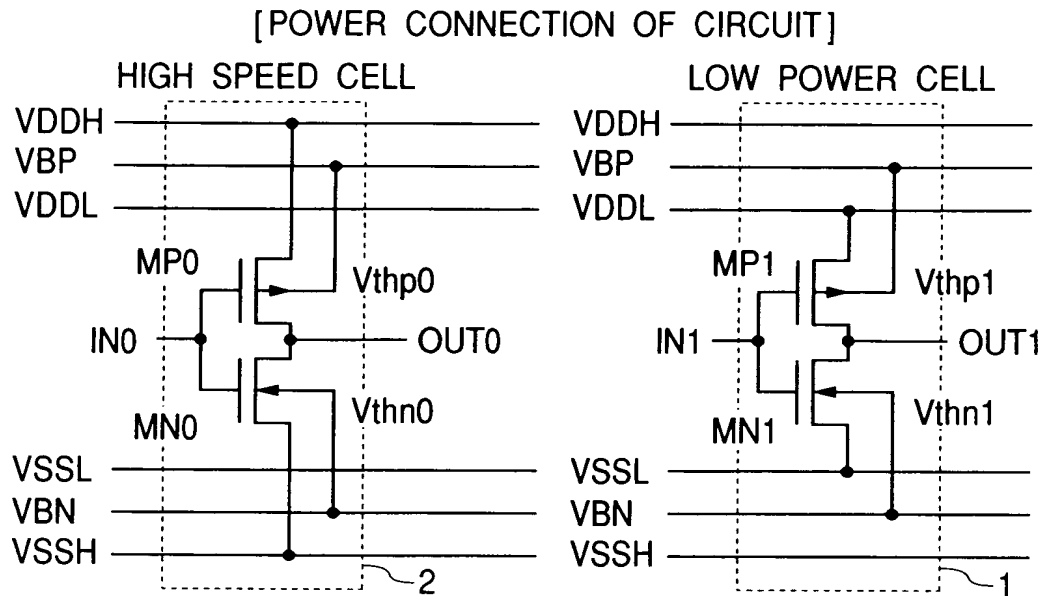
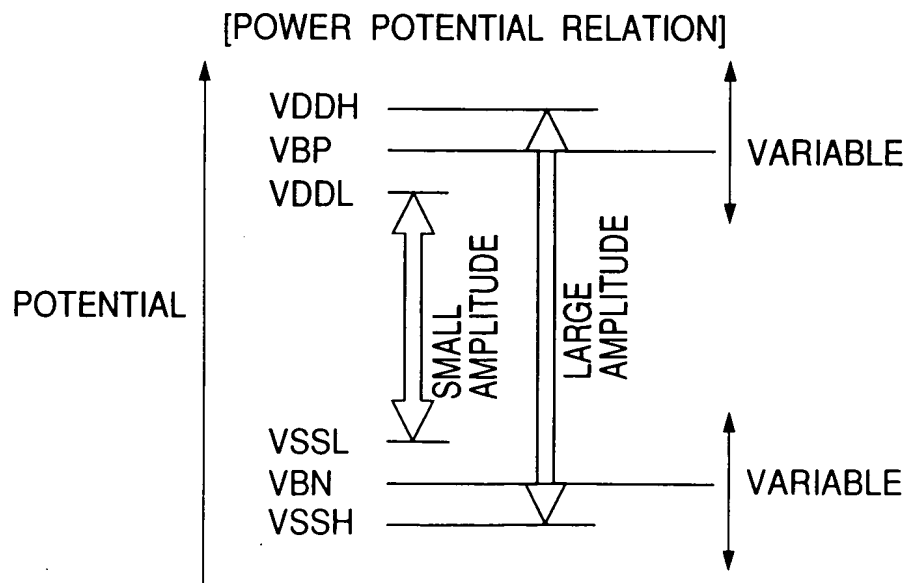
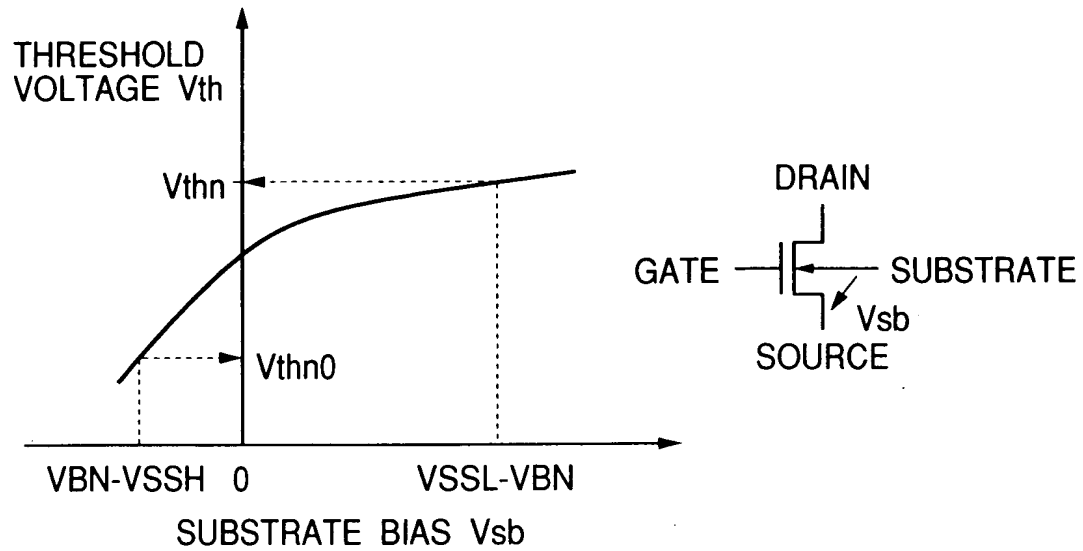
FIG. 1**FIG. 2**

FIG. 3

[INCREASE IN THRESHOLD VOLTAGE BY APPLICATION OF SUBSTRATE BIAS]

**FIG. 4**

[DECREASE IN LEAK CURRENT BY INCREASE IN THRESHOLD VOLTAGE]

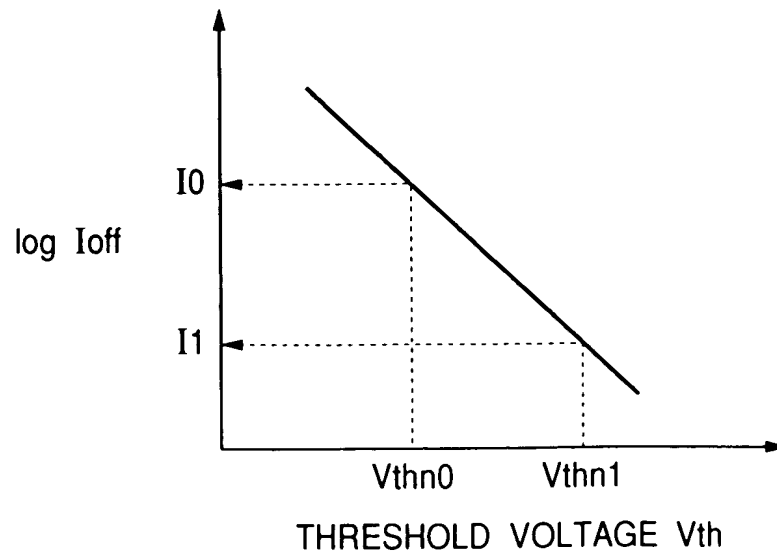


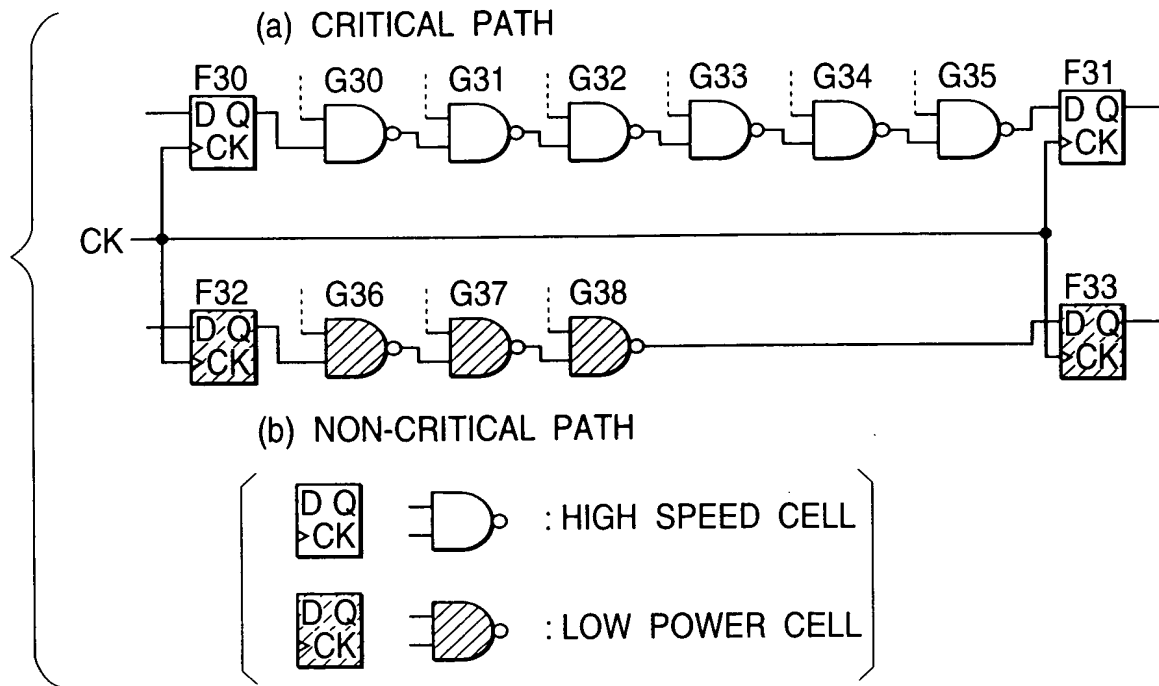
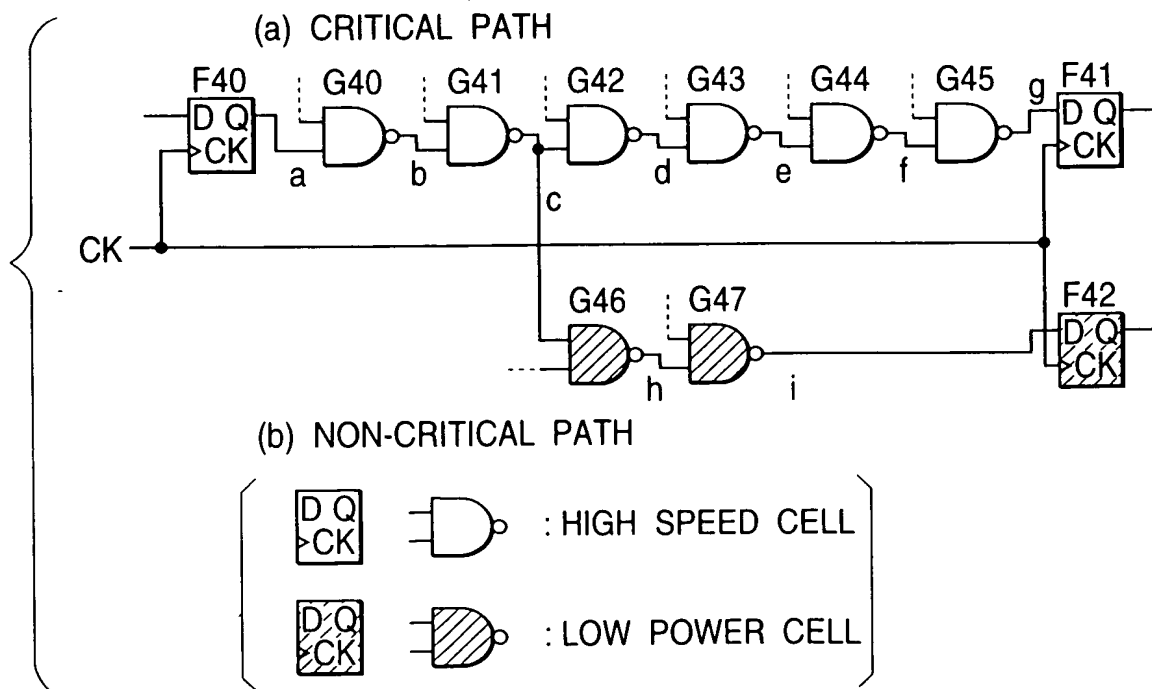
FIG. 5**FIG. 6**

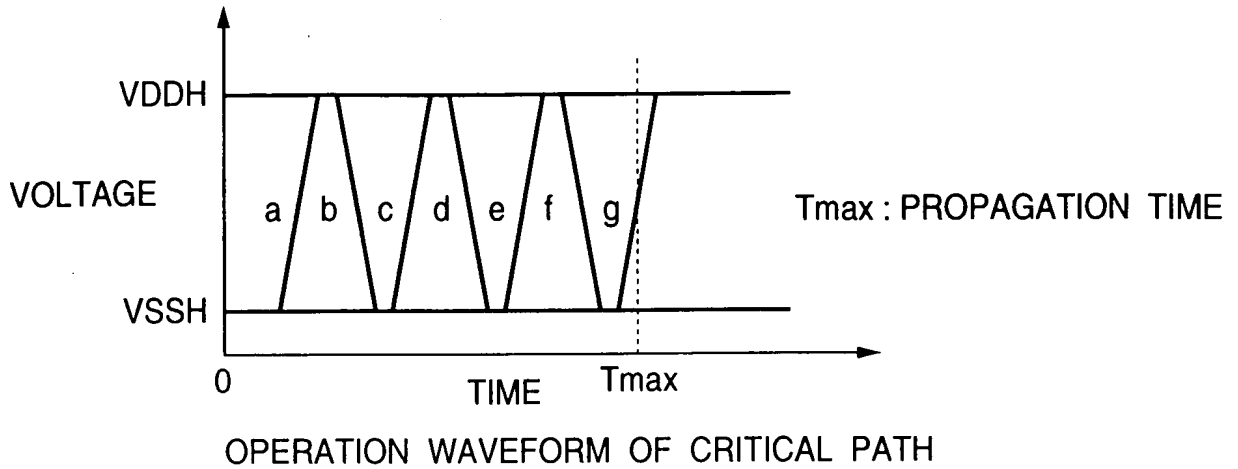
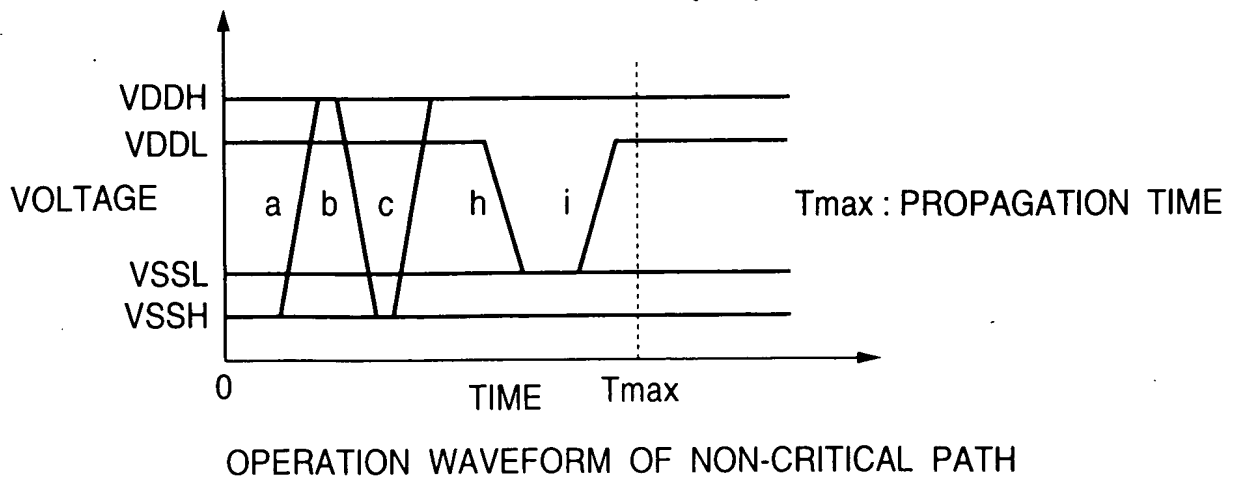
FIG. 7(A)**FIG. 7(B)**

FIG. 8

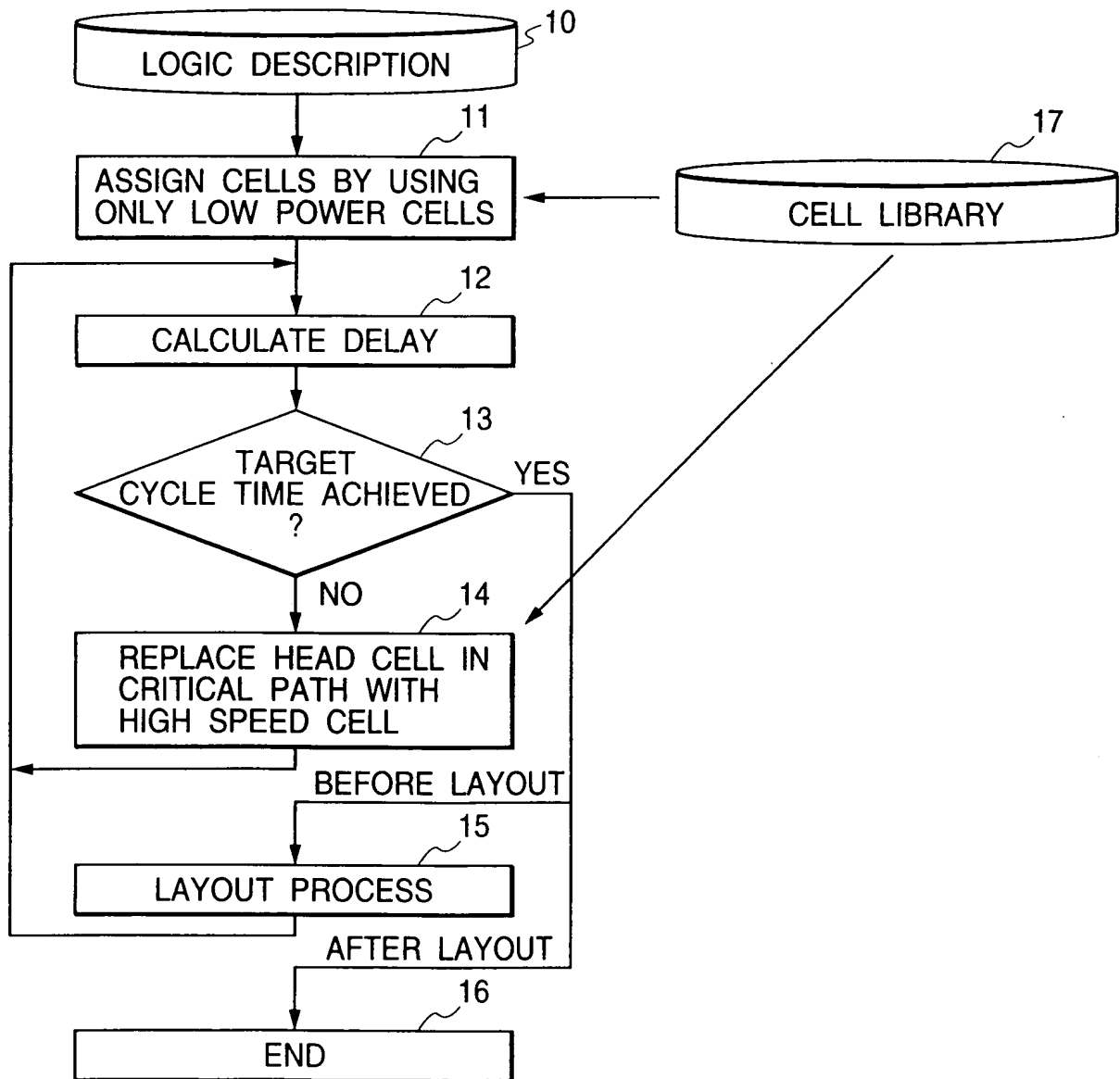


FIG. 9(A)

[CASE USING ONLY LOW POWER CELLS]

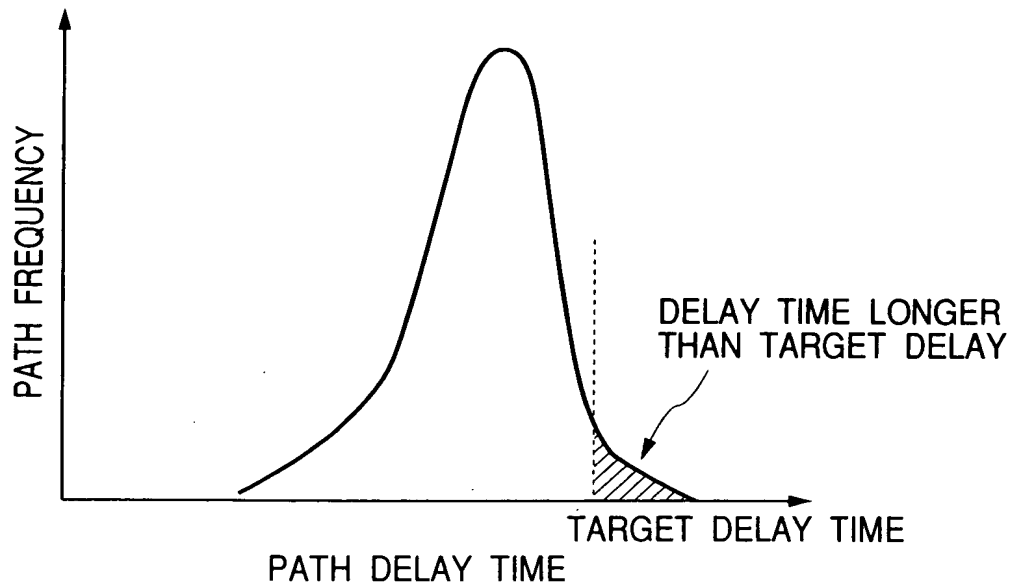


FIG. 9(B)

[CASE USING HIGH SPEED CELL FOR CRITICAL PATH]

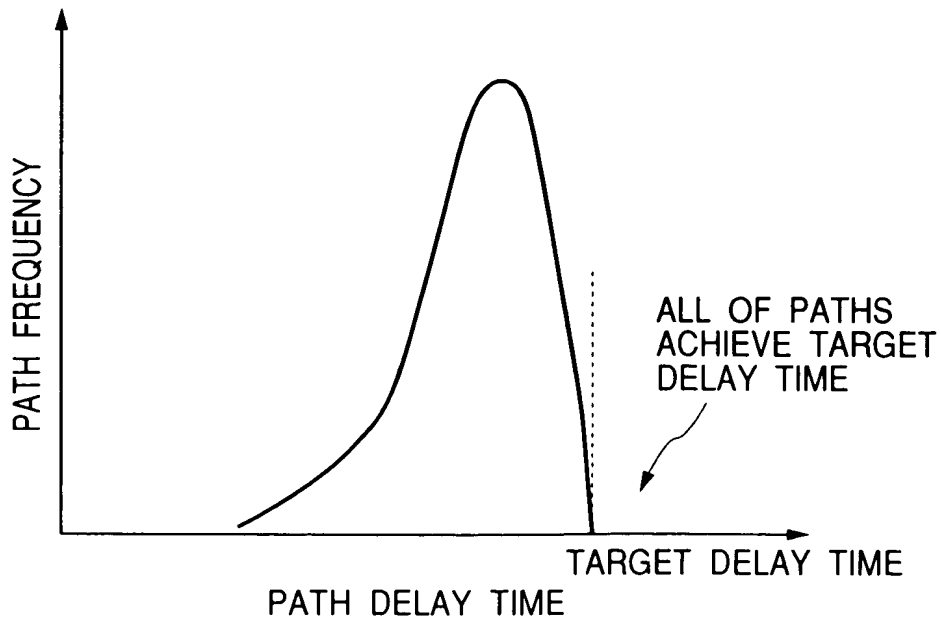


FIG. 10(A)

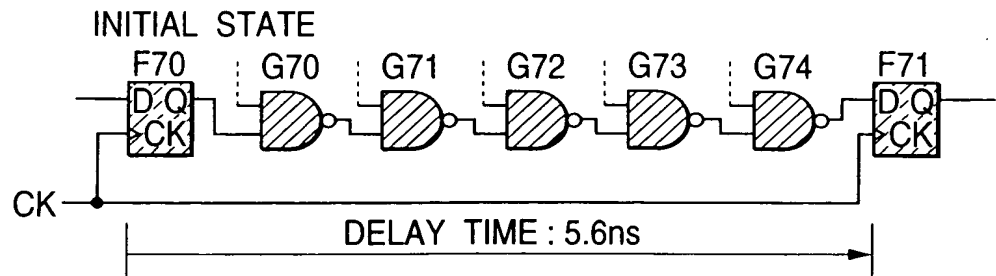


FIG. 10(B)

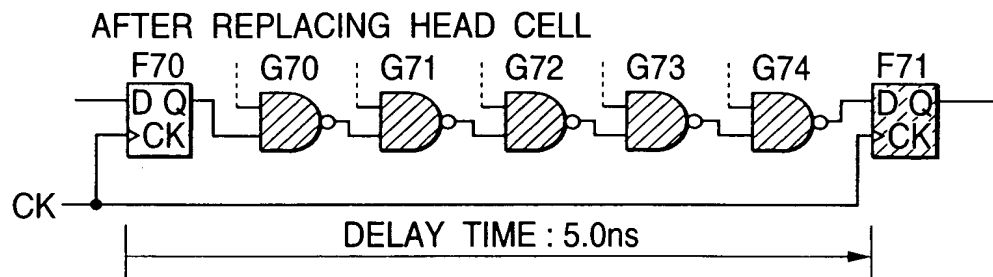


FIG. 10(C)

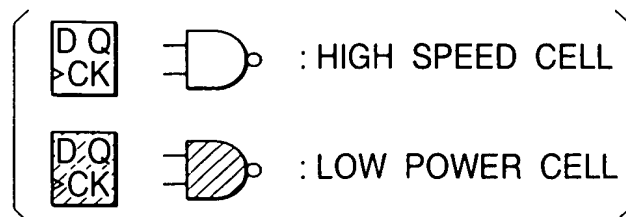
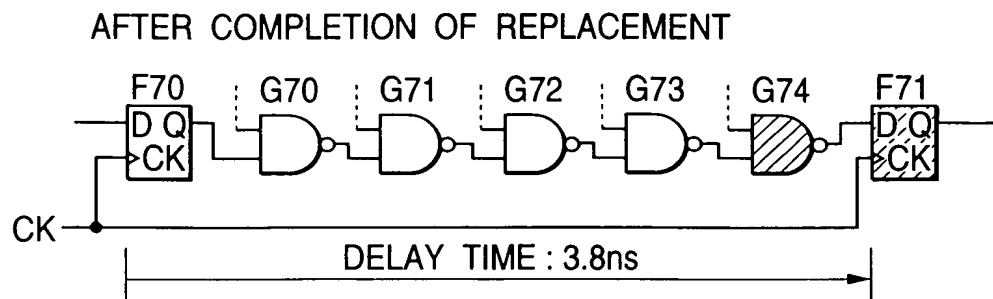


Figure 1 illustrates a logic circuit with level shifting. The circuit includes a clock signal CK, several flip-flops (F80, F81, F82, F83), and logic gates (G80, G81, G82, G83, G84, G85, G86). The circuit is designed to shift the clock level for a subset of components. A legend at the bottom defines the symbols:

- : HIGH SPEED CELL
- : LOW POWER CELL
- : FLIP FLOP WITH LEVEL SHIFTING FUNCTION

FIG. 12

[FLIP FLOP WITH LEVEL SHIFTING FUNCTION]

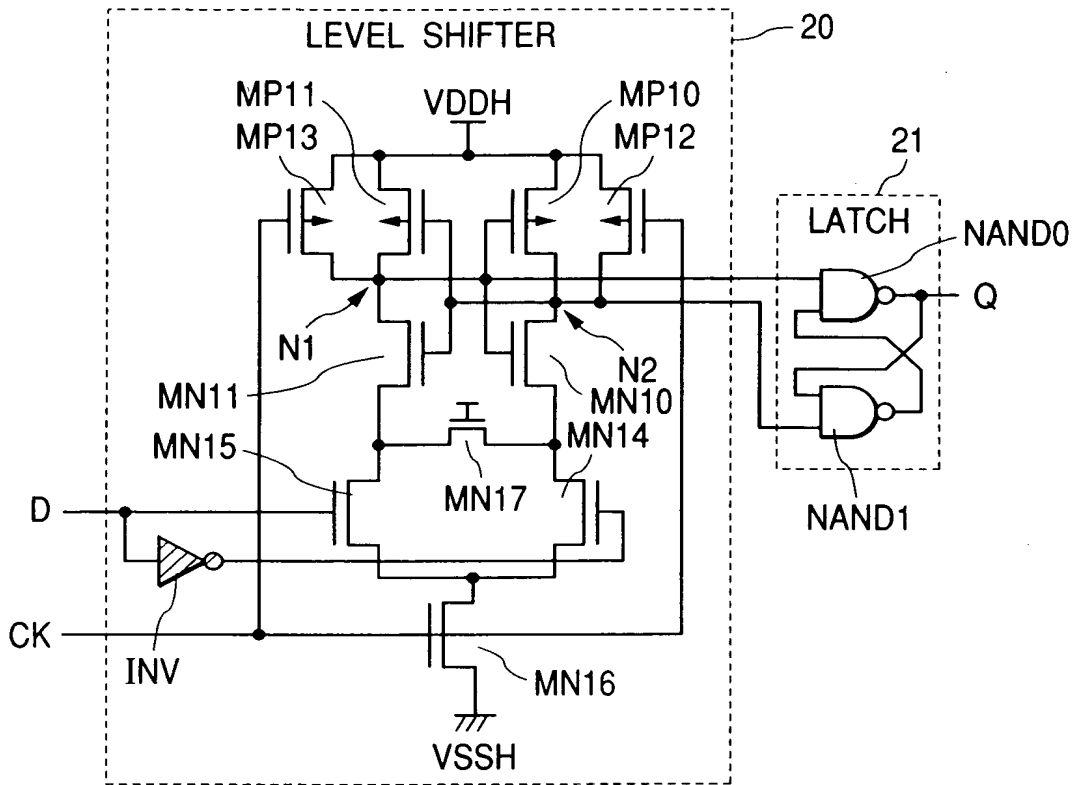
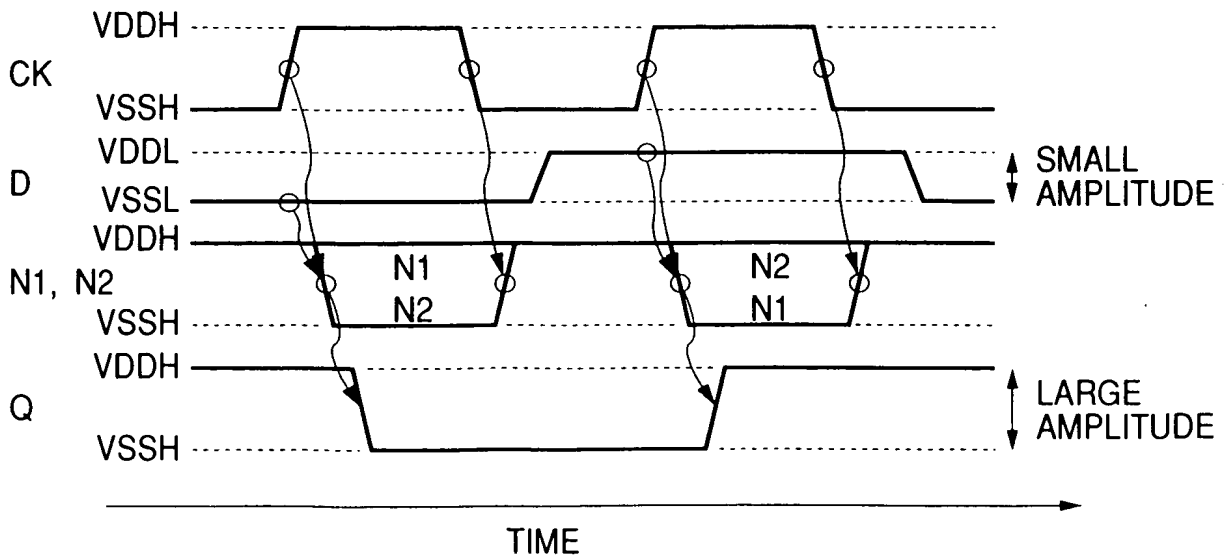
**FIG. 13**

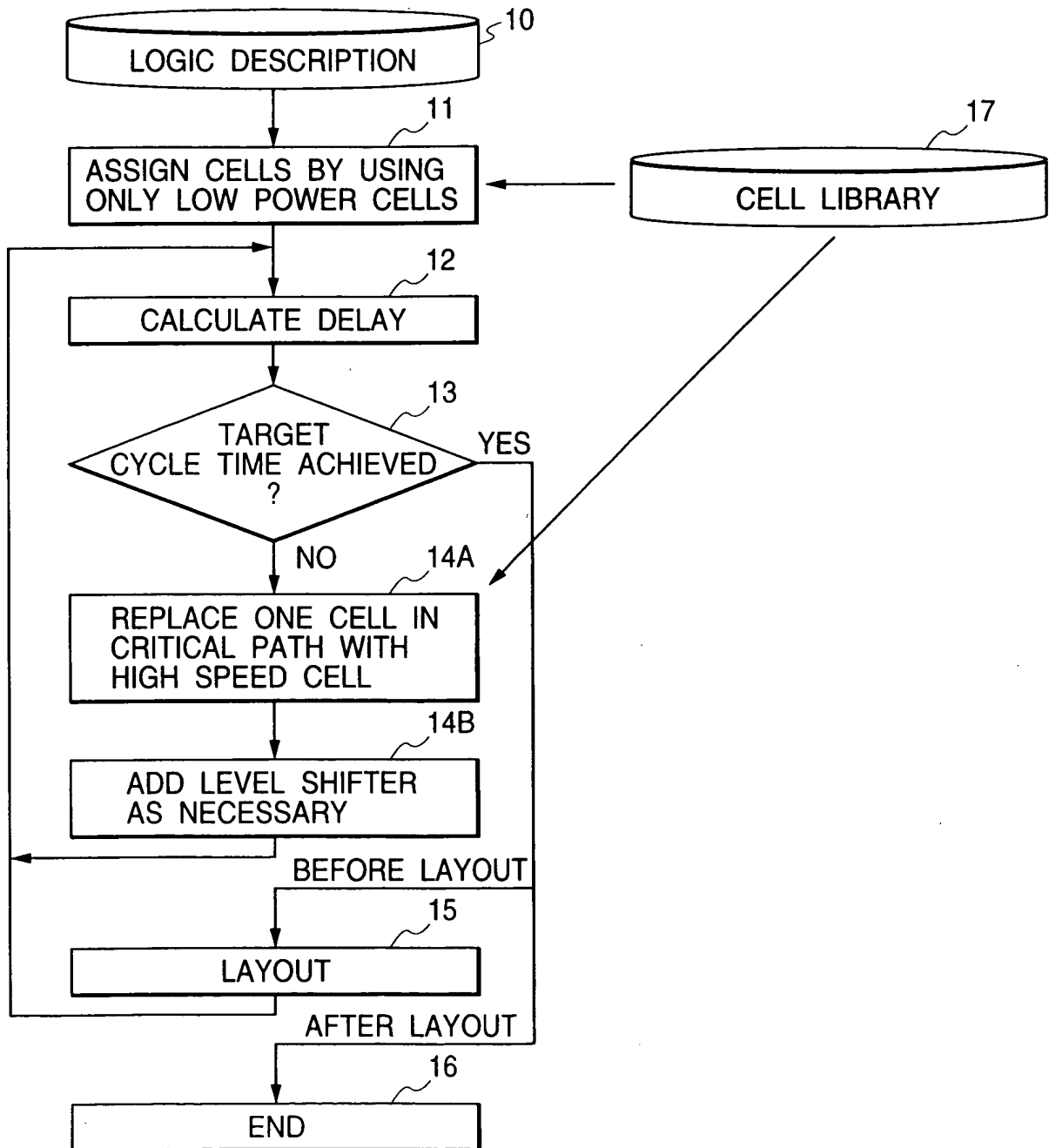
FIG. 14

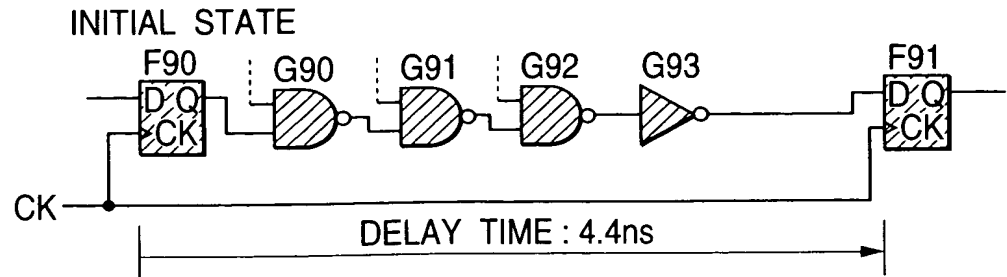
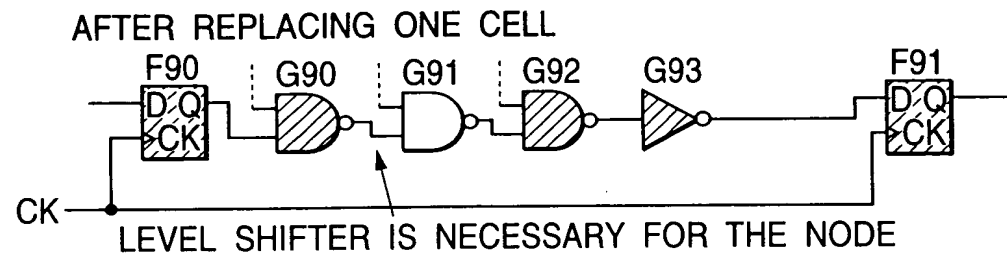
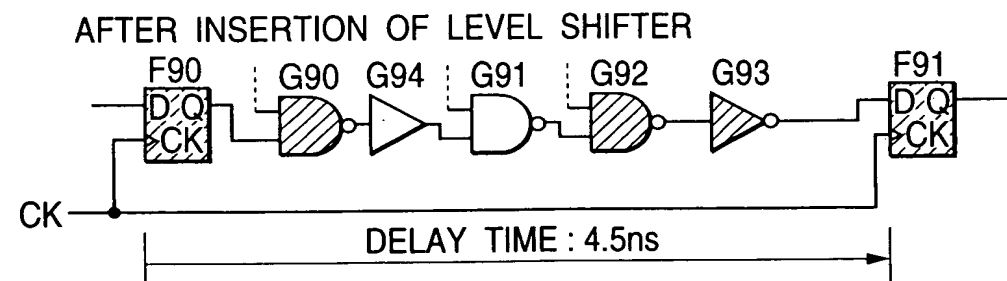
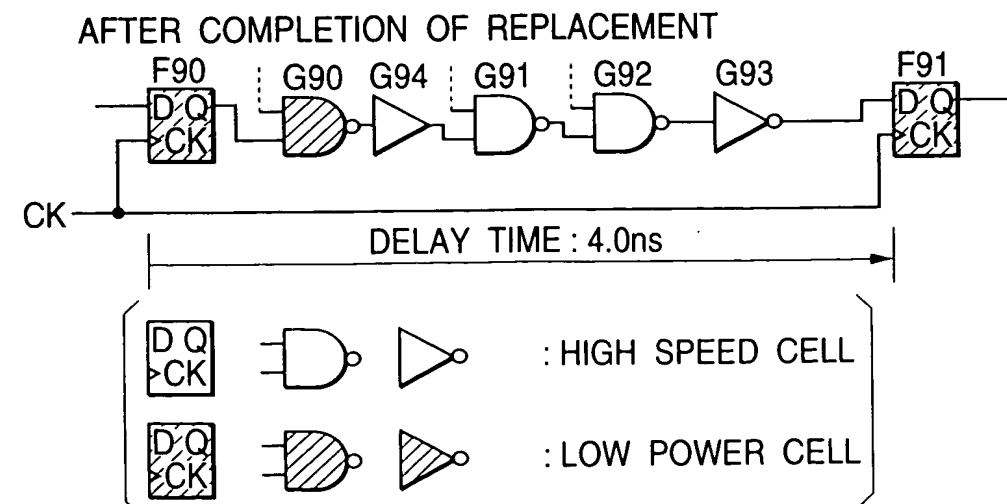
FIG. 15(A)**FIG. 15(B)****FIG. 15(C)****FIG. 15(D)**

FIG. 16

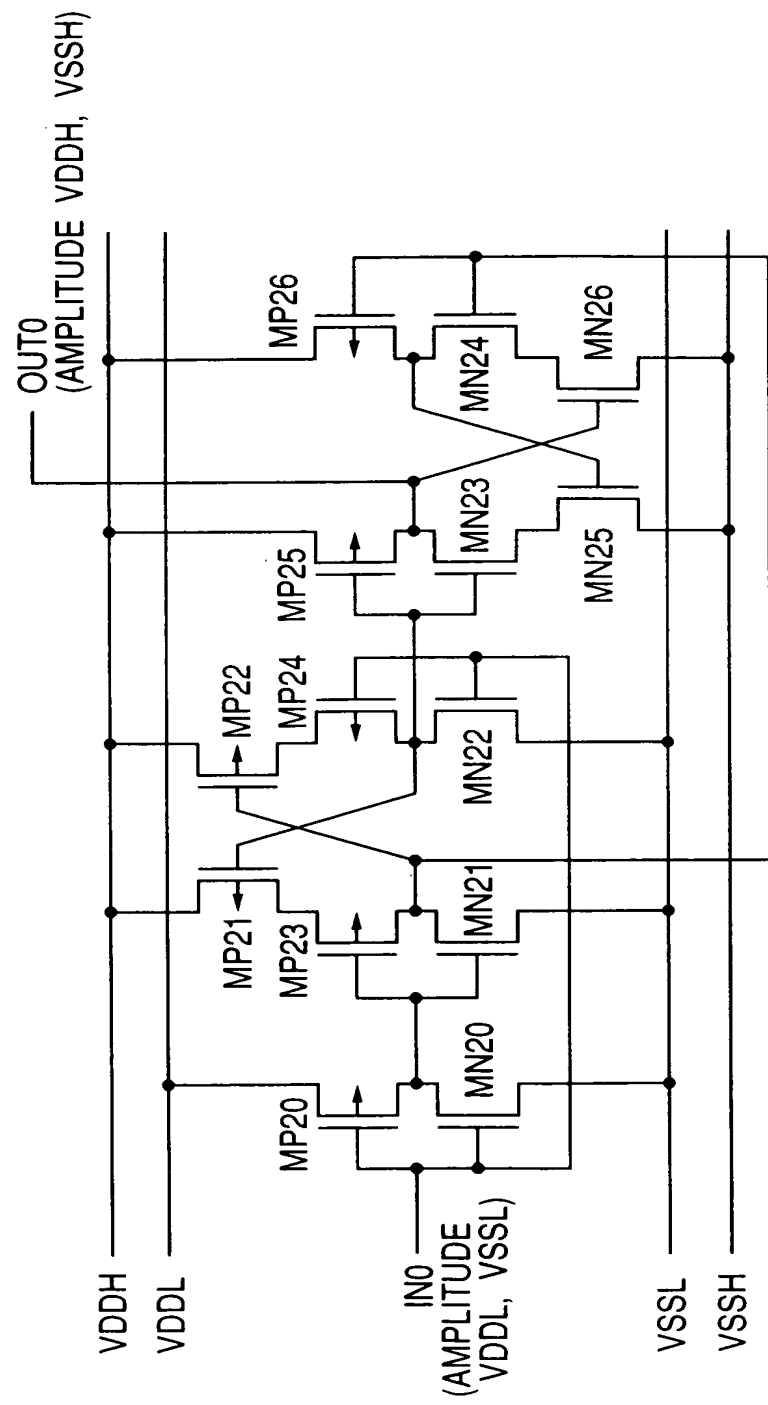


FIG. 17

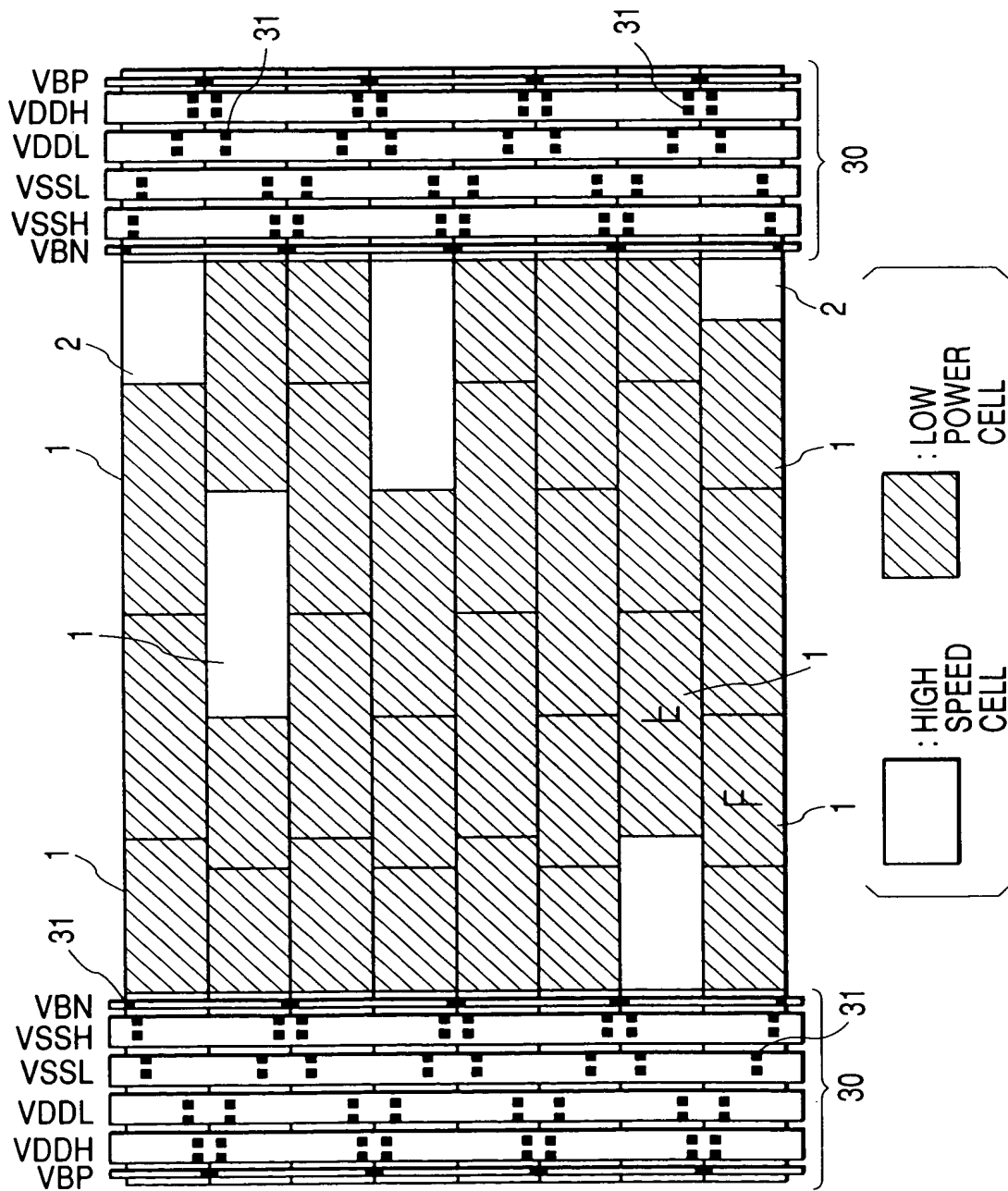


FIG. 18

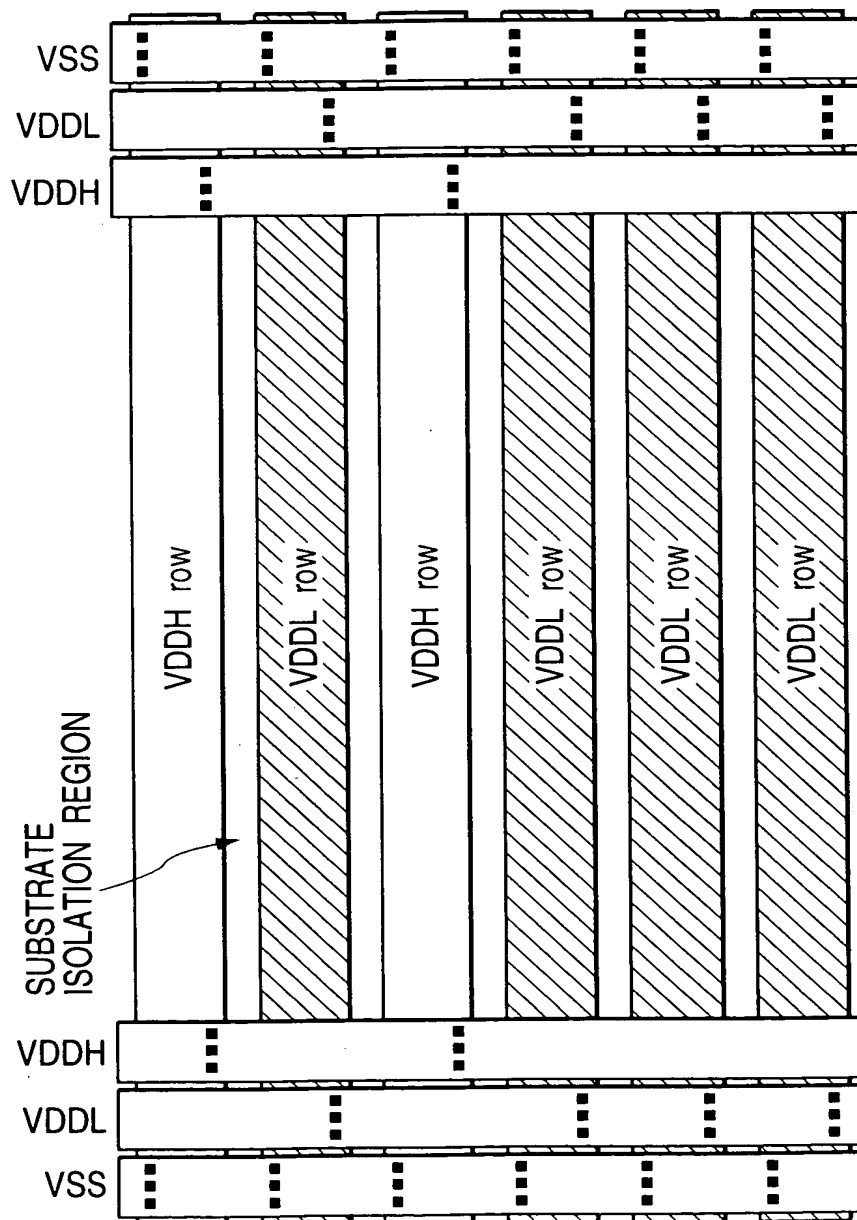


FIG. 19(A)

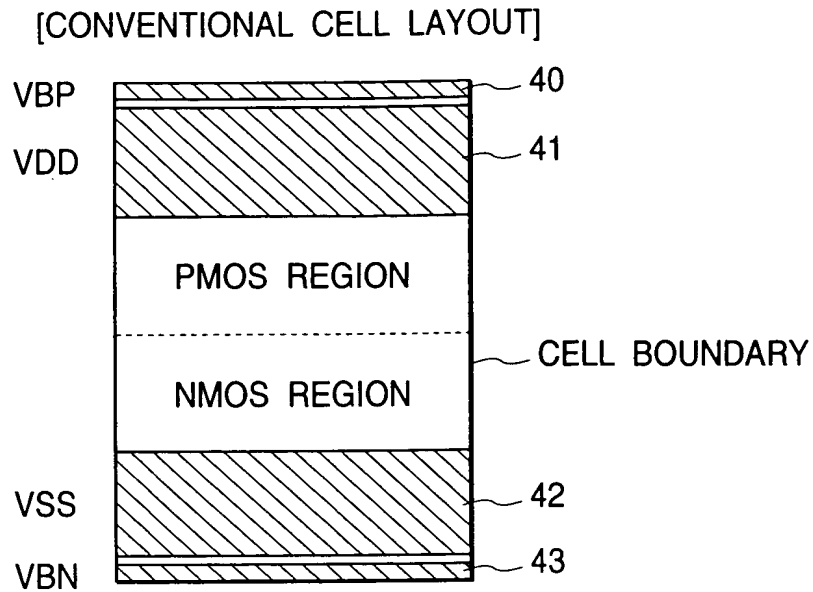


FIG. 19(B)

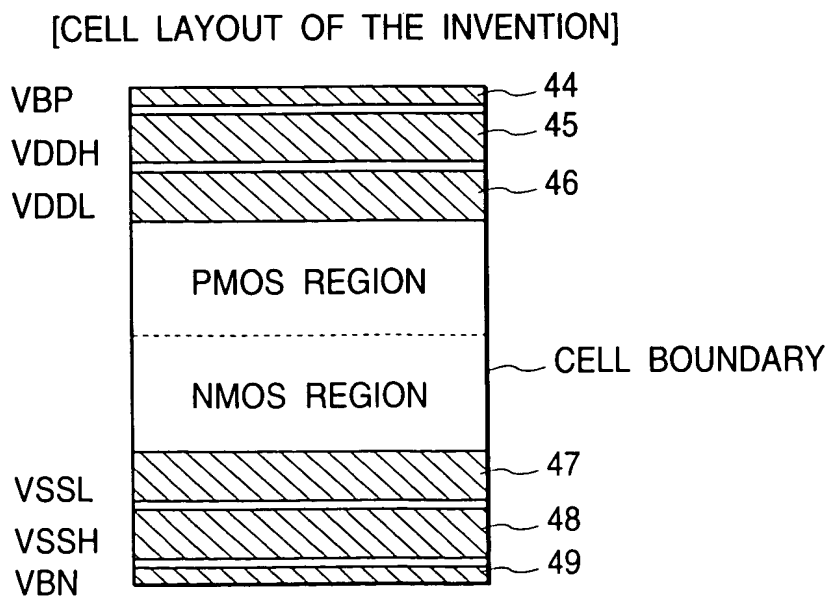


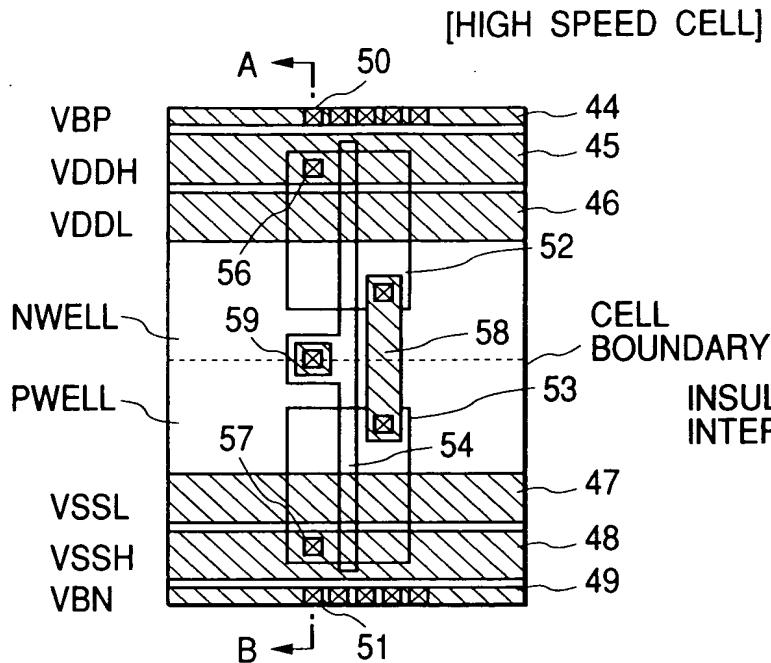
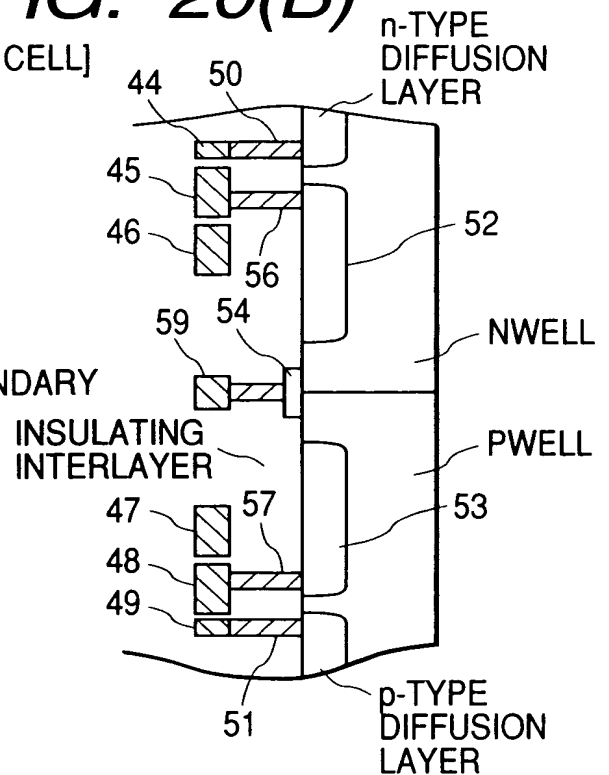
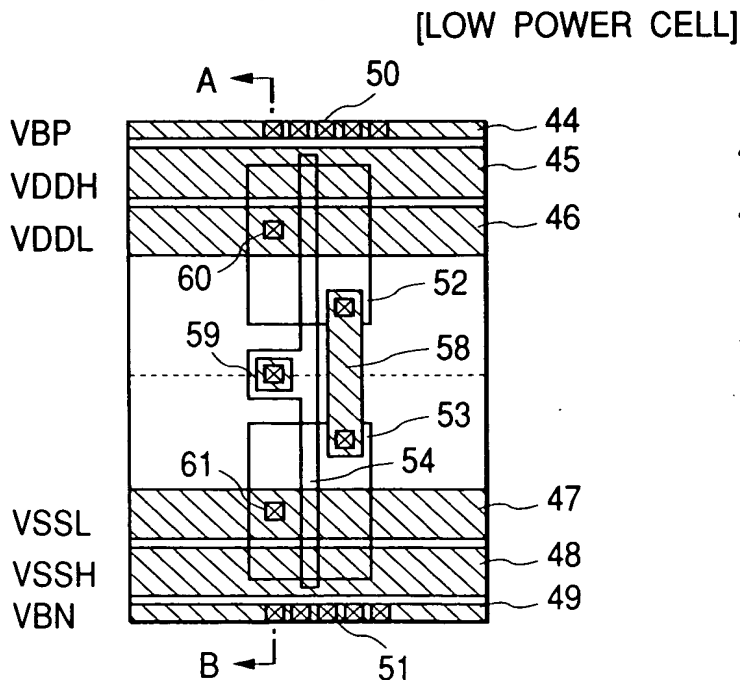
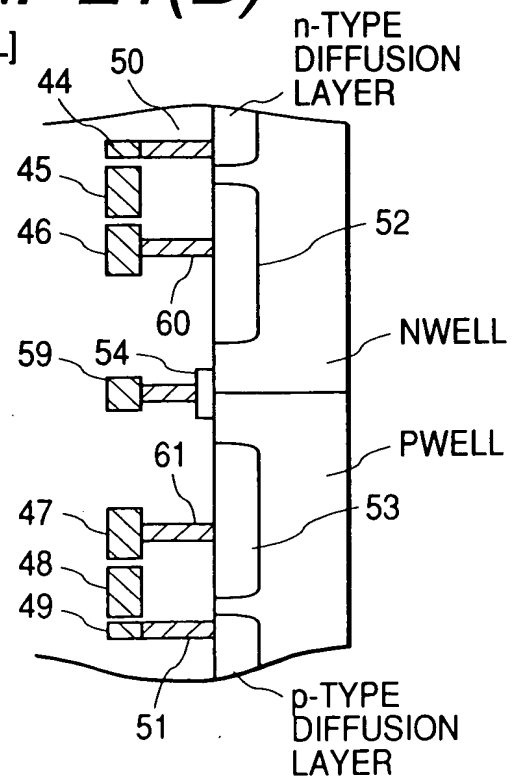
FIG. 20(A)**FIG. 20(B)****FIG. 21(A)****FIG. 21(B)**

FIG. 22

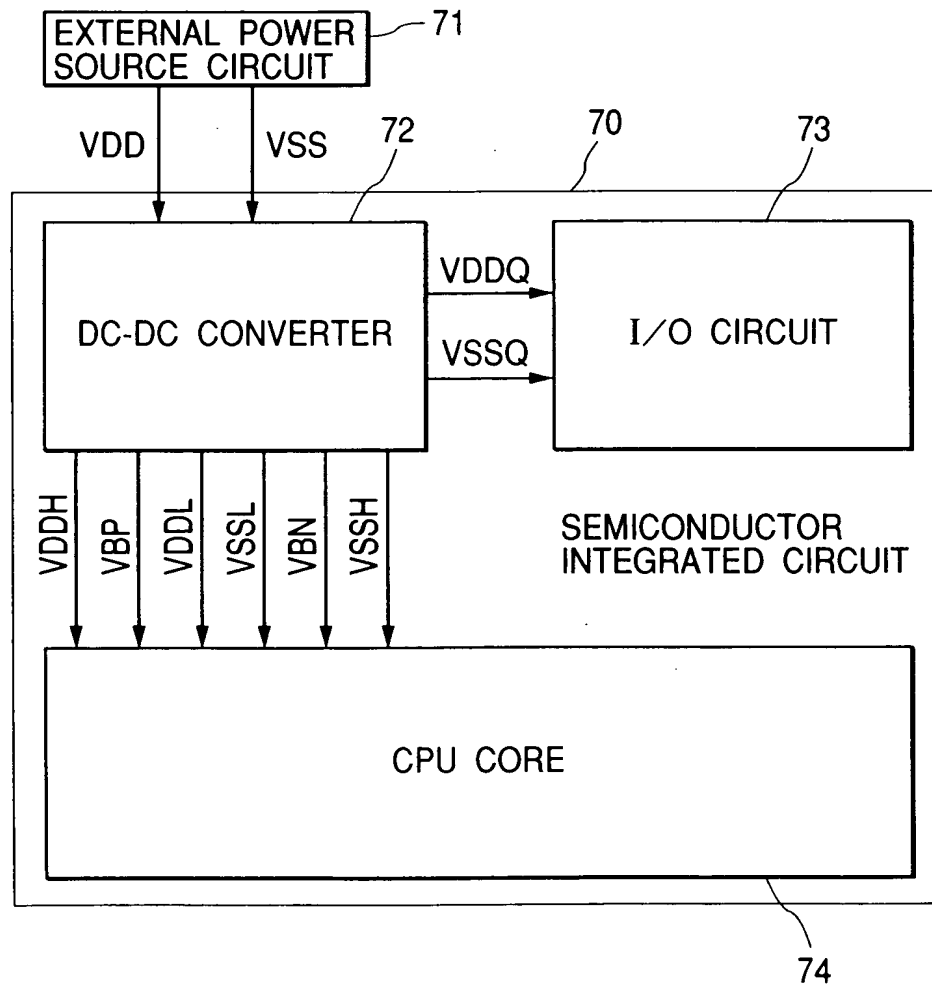


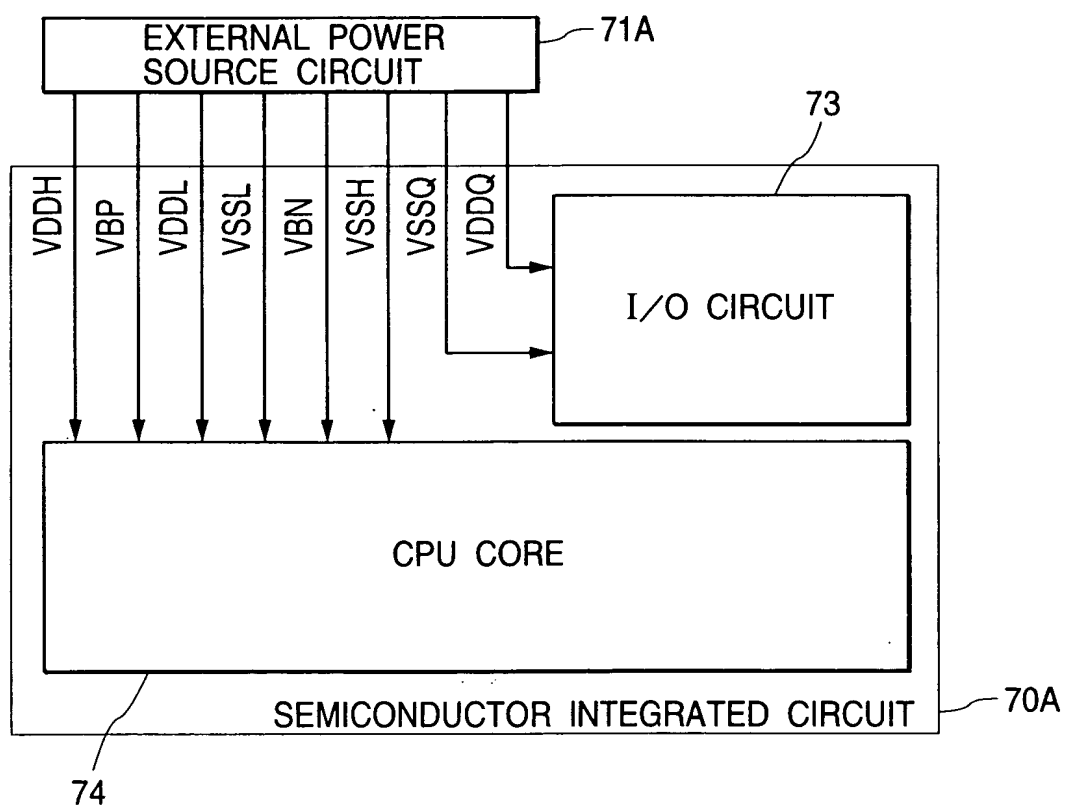
FIG. 23

FIG. 24

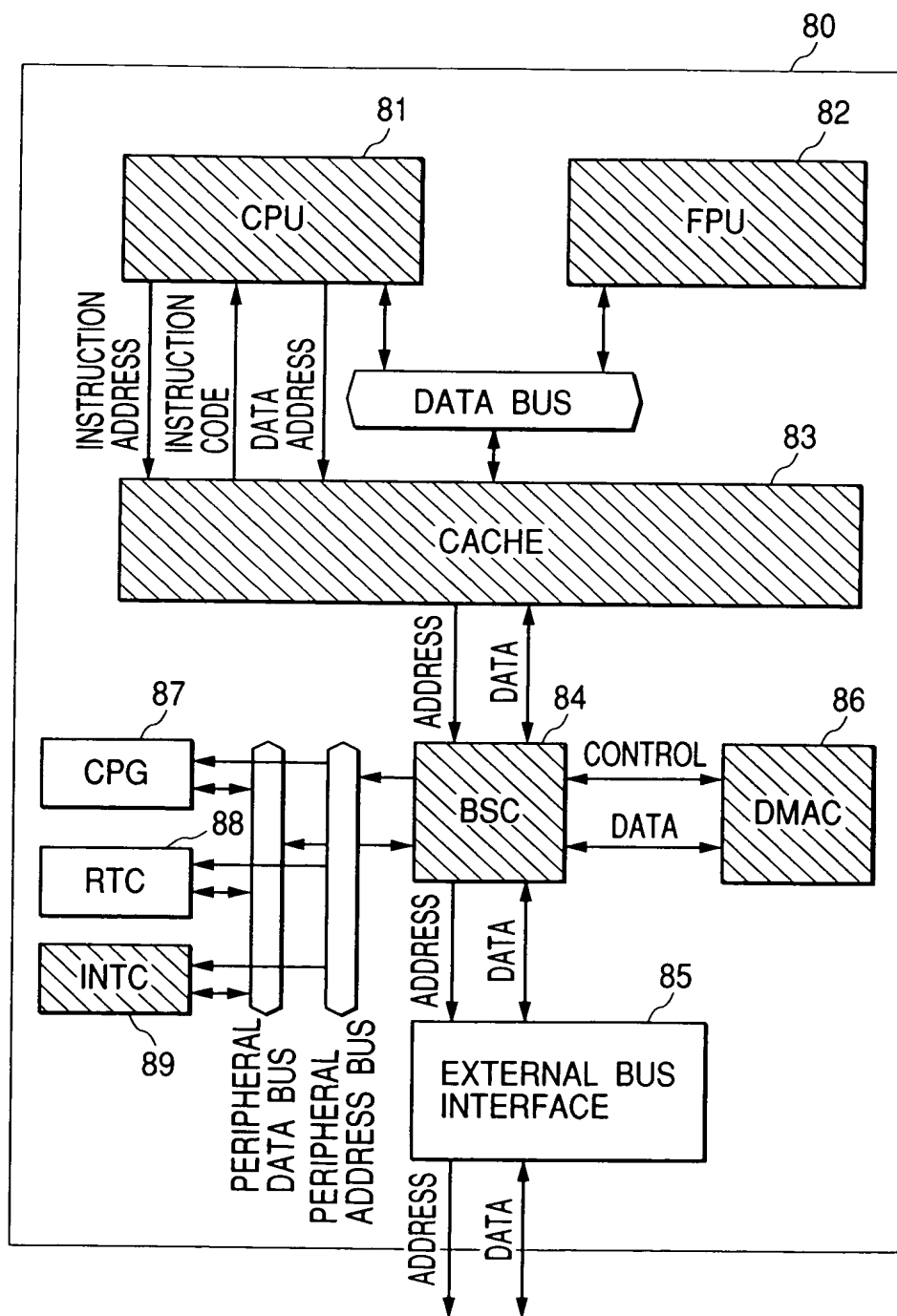


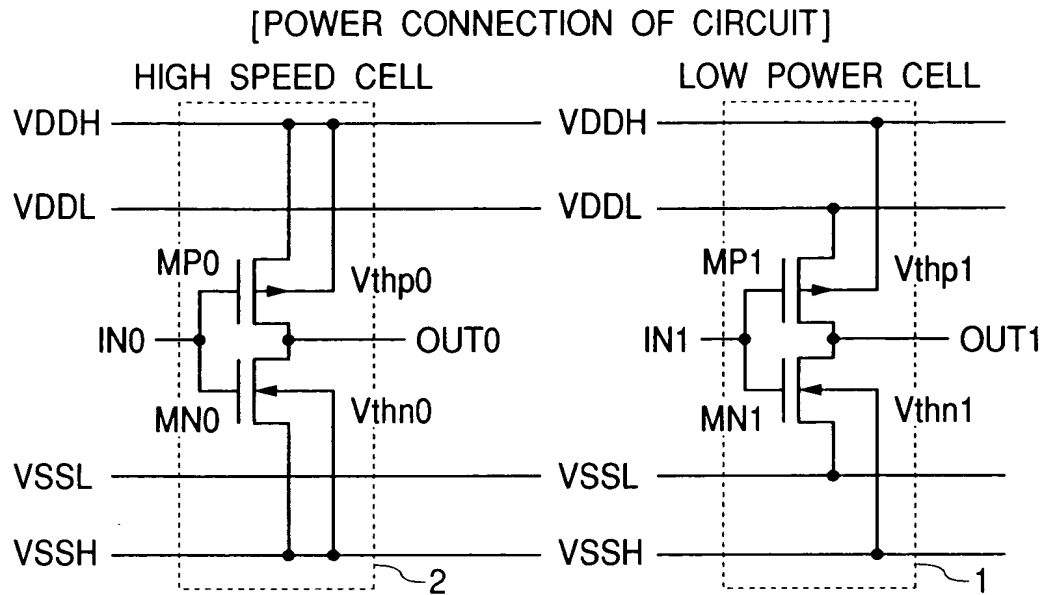
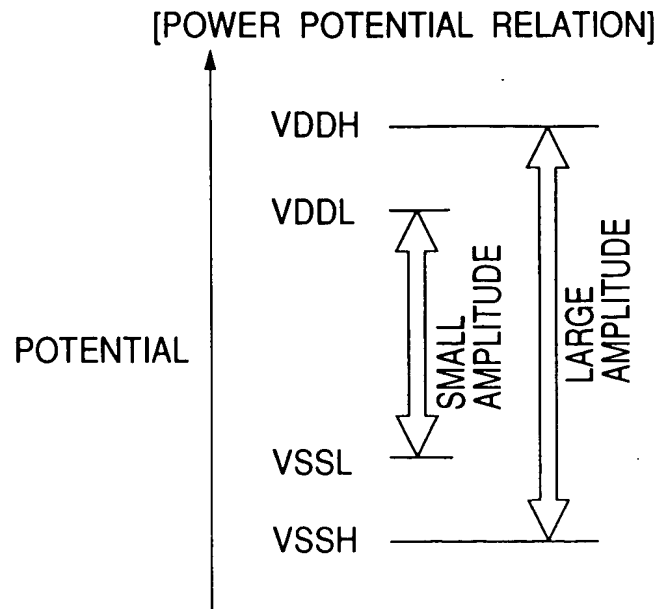
FIG. 25**FIG. 26**

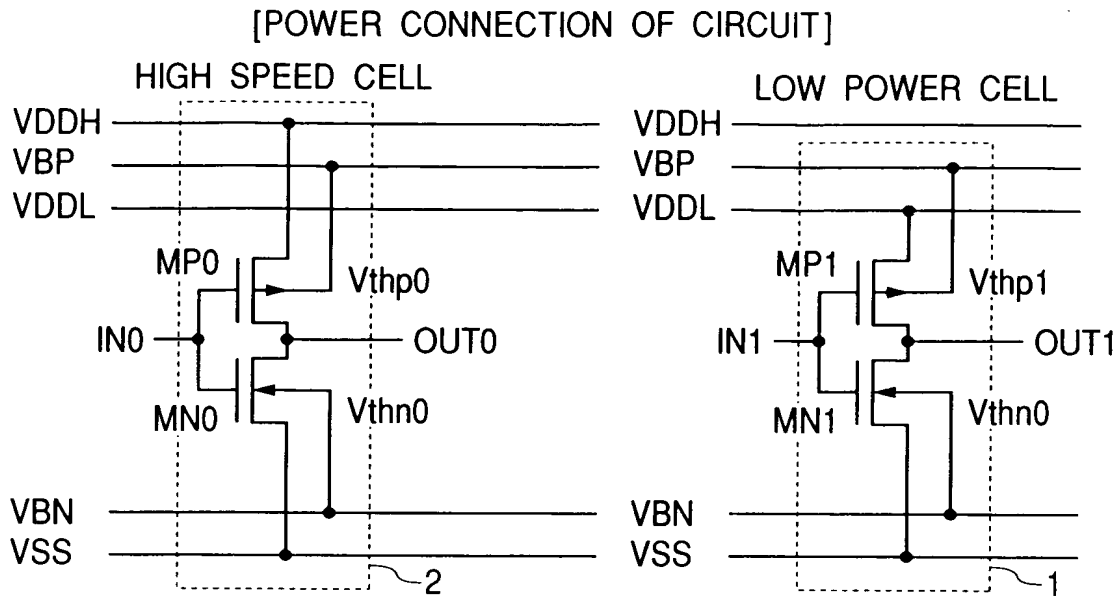
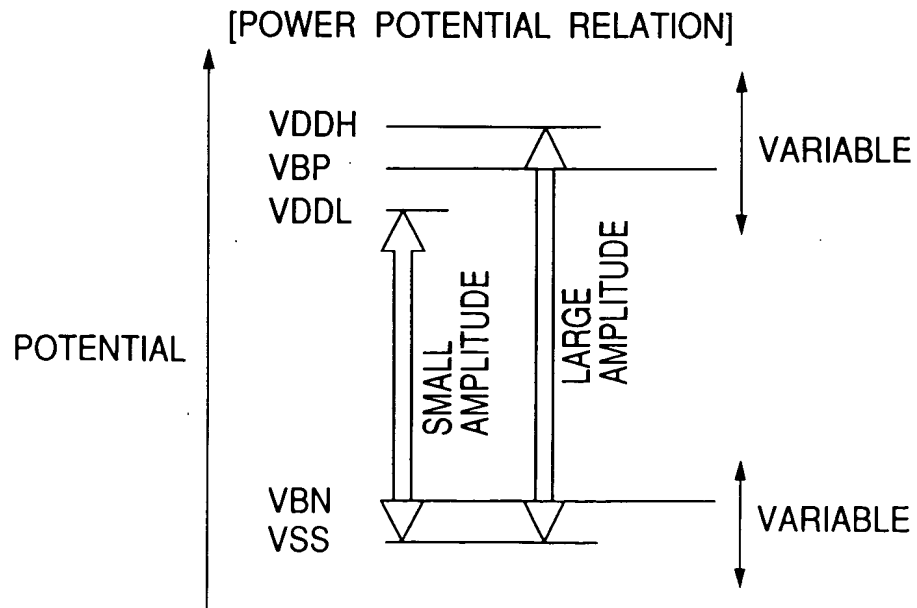
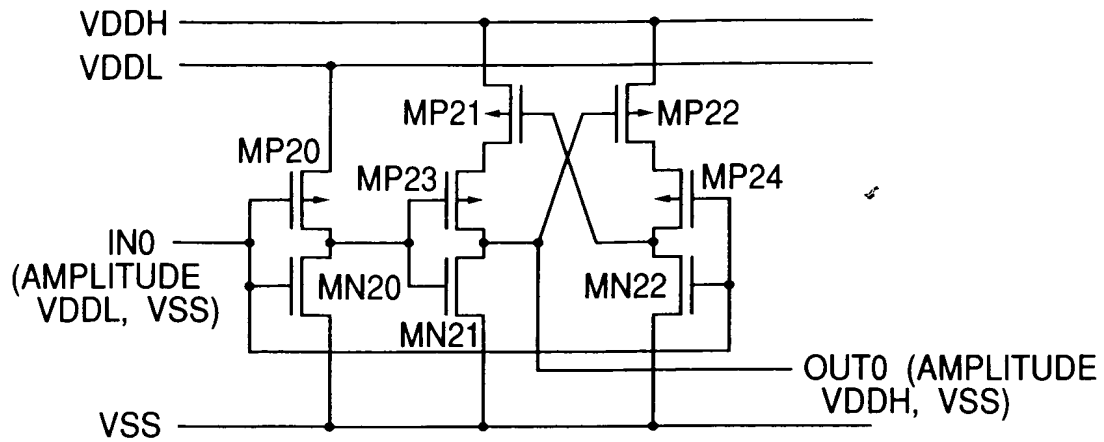
FIG. 27**FIG. 28**

FIG. 29**FIG. 30**